8051 family warm boot determinations AN424

DESCRIPTION

For some classes of applications, it may be desirable to know if the application of the reset signal to a microcontroller is due to an initial power-on sequence, or is the result of an external signal such as an operator pressing a reset pushbutton, or the result of a watchdog timer or similar event.

While there are perhaps numerous hardware solutions that can be employed, a simple software solution can offer a high degree of confidence in making this determination. The task is to determine the differences in state of resources internal to the microcontroller that would occur as a result of these two types of reset conditions. With respect to the 80C51 family of microcontrollers, on-chip resources consist of the special function registers (SFRs) and the internal data memory (RAM). Most of the SFR locations are initialized as a result of a reset condition and thus cannot be used for this determination. The data memory contents are unaffected by reset. Thus, valid data loaded into the RAM of the 80C51 while executing a program would not be affected by the application of an external reset signal provided the power source for the microcontroller has not been removed (as is the case for a “warm boot”).

The contents of data memory as a result of an initial application of power, however, is indeterminate. While this effect has not been extensively characterized, empirical observation suggests that it is highly random in nature. If it is assumed, for the moment, that the behavior of a given byte of data memory is such that it will power-up with a value that is totally random, then there is a one in eight chance that it will power-up with a predetermined value. If the assumption is extended to two bytes, a 16-bit number, then there is one in 2^{16} chance that both bytes will power-up with predetermined values. Extending this to four bytes results in a one in 2^{32} chance; a very small probability. This is the basis for the software determination of a warm or cold boot condition.

The technique consists of evaluating the contents of four consecutive bytes of data memory following a reset condition to determine whether these bytes had been previously loaded with known data values. If the contents of all four bytes match predetermined values, this is interpreted to be a warm boot condition. If there is no match, it is then interpreted to be a cold boot condition. At this point, it is necessary to load these four bytes with predetermined data to prepare for the possibility of a subsequent warm boot condition.

The software example included in this application brief can be used to perform this warm or cold boot determination.

The symbols WARM1 thorough WARM4 represent the predetermined values. The symbol WARM is the address of the first of the four consecutive bytes in data memory. It is set to 30H to avoid conflict with the four register banks, the stack, and the bit-addressable locations in data memory. The symbol WARMBT is a bit-addressable location used as a status bit. It is set as the result of a warm boot and cleared as a result of a cold boot.

The label START is the location of the first instruction to be executed following a reset (address = 0000H). An instruction is located here to jump into the main body of the program to bypass the interrupt vector locations.

The main program body begins by loading register R0 with the address of the first byte in data memory to be evaluated. The contents of this first byte is compared with the first predetermined value. If there is no match, the conclusion is that it is a cold boot. However, if a match is found, this does not imply that it is a warm boot since all four bytes must match, and therefore the remaining three bytes must also be evaluated. Register R0 is incremented to point to the second byte and then compared to the second predetermined value. Comparison of the bytes proceeds until either a no match condition is found or until all four bytes have been evaluated successfully. If all four bytes compared favorable, then a status bit (WARMBT) is set to indicate a warm boot and the remainder of the application program is completed.

An unsuccessful comparison results in branching to the label COLD. This section of code clears the status bit (WARMBT) to indicate a cold boot, and loads the four bytes of data memory with the predetermined values preparing the system for a subsequent possible warm boot. Program flow then continues with the remainder of the application program.

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                      1
                      2    ;warm boot application example
                      3
  0030                4    WARM    EQU     30H             ;first location of the four bytes in RAM
  0055                5    WARM1   EQU     55H             ;first predetermined value
  00AA                6    WARM2   EQU     0AAH            ;second predetermined value
  0033                7    WARM3   EQU     33H             ;third predetermined value
  00CC                8    WARM4   EQU     0CCH            ;fourth predetermined value
  0000                9    WARMBT  EQU     0               ;warm boot status bit
                     10
0000                 11            ORG     0
                     12
0000 020026          13    START:  JMP     MAIN            ;bypass interrupt vectors
                     14
0026                 15            ORG     26H
                     16
0026 7830            17    MAIN:   MOV     R0,#WARM        ;pointer for first byte
0028 B65511          18            CJNE    @R0,#WARM1,COLD ;test first byte
002B 08              19            INC     R0              ;pointer for second byte
002C B6AA0D          20            CJNE    @R0,#WARM2,COLD ;test second byte
002F 08              21            INC     R0              ;pointer for third byte
0030 B63309          22            CJNE    @R0,#WARM3,COLD ;test third byte
0033 08              23            INC     R0              ;pointer for fourth byte
0034 B6CC05          24            CJNE    @R0,#WARM4,COLD ;test fourth byte
0037 D200            25            SETB    WARMBT          ;this is a warm start
0039 02004B          26            JMP     INIT            ;continue with rest of application
003C C200            27    COLD:   CLR     WARMBT          ;this is a cold boot
003E 7830            28            MOV     R0,#WARM        ;pointer for first byte
0040 7655            29            MOV     @R0,#WARM1      ;load the four bytes for future test
0042 08              30            INC     R0              ;
0043 76AA            31            MOV     @R0,#WARM2      ;
0045 08              32            INC     R0              ;
0046 7633            33            MOV     @R0,#WARM3      ;
0048 08              34            INC     R0              ;
0049 76CC            35            MOV     @R0,#WARM4      ;
004B                 36    INIT:                           ;continue with the application
                     37
                     38    END

ASSEMBLY COMPLETE, 0 ERRORS FOUND

COLD . . . . . .  C ADDR  003CH
INIT . . . . . .  C ADDR  004BH
MAIN . . . . . .  C ADDR  0026H
START. . . . . .  C ADDR  0000H  NOT USED
WARM . . . . . .    NUMB  0030H
WARM1. . . . . .    NUMB  0055H
WARM2. . . . . .    NUMB  00AAH
WARM3. . . . . .    NUMB  0033H
WARM4. . . . . .    NUMB  00CCH
WARMBT . . . . .    NUMB  0000H
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